IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	: David Qiang Meng	Art Unit	: 2187
Serial No.	: 10/750,423	Examiner	: Jared Ian Rutz
Filed	: December 30, 2003	Conf. No.	: 4620
Title	: PARTITIONING MEMORY		

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APPEAL BRIEF ON BEHALF OF DAVID QIANG MENG

Please charge the brief fee of $500 to Deposit Account No. 06-1050.

(1) Real Party in Interest

The real party in interest in the above application is Intel Corporation.

(2) Related Appeals and Interferences

The Appellant is not aware of any appeals or interferences related to the above-identified patent application.

(3) Status of Claims

This is an appeal from the decision of the Examiner in an Office Action dated October 18, 2006, rejecting claims 1-26, all of the claims of the above application, and from the decision of the Pre-Appeal Brief Review Panel, dated March 13, 2007, which concluded that the current case should proceed to appeal.

The claims have been twice rejected. Claims 1-26 are the subject of this appeal.

(4) Status of Amendments

All amendments have been entered. Appellant filed a Notice of Appeal on January 18, 2007.

(5) Summary of Claimed Subject Matter

Claim 1

One aspect of Appellant's invention is set out in claim 1, as a computer implemented method. "Referring to FIG. 1, a system 10 for transmitting packets from a computer system 12 through a network 14 *** to other computer systems 16, 18 by way of another network 20 includes a router 22 that collects a stream of "n" packets 24 and schedules delivery to the appropriate destinations of the individual packets as provided by information included in the packets." [Specification, page 2, lines 13-20]

Inventive features of claim 1 include partitioning a memory device to produce a first group of memory entries being accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in parallel. "Each of the entries

in CAM 54 is configurable by a CAM manager 58 that is implemented as microcode in the control store 50 and, which is executed by the packet engine 48. The CAM manager 58 partitions the CAM 54 into a particular number of entries." [Specification, page 9, lines 18-22] "CAM 54 allows the entries to be accessed in parallel so that all or some of the entries can be checked during the same time period (e.g., clock cycle) to determine if particular data is present in one of the entries." [Specification, page 8, lines 7-11].

Claim 8

Claim 8 recites another aspect of the invention. Claim 8 is a computer program product, tangibly embodied in a computer readable medium. "Instructions executed on packet engine 48 are typically written in microcode. However, in some arrangements, high-level languages such as "C", "C++", or other similar computer languages are used to program instructions for execution on packet engine 48. The packet engine 48 includes a control store 50 that stores one or more blocks of microcode instructions, which are referred to as microblocks and are executed on the packet engine 48." [Specification, page 7, line 12-19]

Inventive features of claim 8 include the computer program product being operable to cause a machine to partition a memory device to produce a first group of memory entries being accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in parallel. "Each of the entries in CAM 54 is configurable by a CAM manager 58 that is implemented as microcode in the control store 50 and, which is executed by the packet engine 48. The CAM manager 58 partitions the CAM 54 into a particular number of entries." [Specification, page 9, lines 18-22] Also, "CAM 54 allows the entries to be accessed in parallel so that all or some of the entries can be checked during the same time period (e.g., clock cycle) to determine if particular data is present in one of the entries." [Specification, page 8, lines 7-11]

Claim 15

Claim 15 is directed to a content-addressable memory (CAM) manager. "Each of the entries in CAM 54 is configurable by a CAM manager 58 that is implemented as microcode in

the control store 50 and, which is executed by the packet engine 48." [Specification, page 9, lines 18-20]

Inventive features of Appellant's claim 15 include a process to partition a memory device to produce a first group of memory entries being accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in parallel. "For example, CAM 60 (shown in FIG. 4), CAM 70 (shown in FIG. 5), and CAM 80 (shown in FIG. 6) are partitioned by CAM manager 58 into sixteen entries while CAM 90 (shown in FIG. 7) is partitioned into thirty-two entries." [Specification, page 14, line 20, to page 15, line 2] "CAM 54 allows the entries to be accessed in parallel so that all or some of the entries can be checked during the same time period (e.g., clock cycle) to determine if particular data is present in one of the entries." [Specification, page 8, lines 7-11]

Claim 18

Claim 18 is directed to a system. "Referring to FIG. 1, a system 10 for transmitting packets from a computer system 12 through a network 14 (e.g., a local area network (LAN), a wide area network (WAN), the Internet, etc.) to other computer systems 16, 18 by way of another network 20 includes a router 22 that collects a stream of "n" packets 24 and schedules delivery to the appropriate destinations of the individual packets as provided by information included in the packets." [Specification, page 2, lines 13-20]

Inventive features of Appellant's claim 18 include a memory device capable of being partitioned to produce a first group of memory entries that is accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in parallel. "To execute arithmetic and logic operations, ALU 52 includes a content-addressable memory (CAM) 54 that includes, e.g., thirty-two entries (i.e., entry 0 – entry 31) that are capable of being used by the packet engine threads to execute microblocks stored in control store 50. CAM 54 allows the entries to be accessed in parallel so that all or some of the entries can be checked during the same time period (e.g., clock cycle) to determine if particular data is present in one of the entries." [Specification, page 8, lines 3-11] "The CAM manager 58 partitions the CAM 54 into a particular number of entries." [Specification, page 9, lines 20-22]

Claim 21

Claim 21 recites another aspect of the invention. Claim 21 is a packet forwarding device. "Referring to FIG. 1, a system 10 for transmitting packets from a computer system 12 through a network 14 (e.g., a local area network (LAN), a wide area network (WAN), the Internet, etc.) to other computer systems 16, 18 by way of another network 20 includes a router 22 that collects a stream of "n" packets 24 and schedules delivery to the appropriate destinations of the individual packets as provided by information included in the packets." [Specification, page 2, lines 13-20]

Inventive features of claim 21 include an input port for receiving a packet. "Typically, the packets are received by the router 22 on one or more input ports 26 that provide a physical link to network 14. The input ports 26 are in communication with a network processor 28 that controls the entering of the incoming packets." [Specification, page 3, lines 3-7]

Inventive features of claim 21 also include an output port for delivering the received packet. "The network processor 28 also communicates with router output ports 30, which are used for scheduling transmission of the packets through network 20 for delivery at one or more appropriate destinations (e.g., computer systems 16, 18)." [Specification, page 3, lines 7-11]

Inventive features of claim 21 also include a memory device capable of being partitioned to produce a first group of memory entries that is accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in parallel. "To execute arithmetic and logic operations, ALU 52 includes a content-addressable memory (CAM) 54 that includes, e.g., thirty-two entries (i.e., entry 0 – entry 31) that are capable of being used by the packet engine threads to execute microblocks stored in control store 50. CAM 54 allows the entries to be accessed in parallel so that all or some of the entries can be checked during the same time period (e.g., clock cycle) to determine if particular data is present in one of the entries." [Specification, page 8, lines 3-11] "The CAM manager 58 partitions the CAM 54 into a particular number of entries." [Specification, page 9, lines 20-22]

Claim 24

Claim 24 is directed to a content-addressable memory (CAM). "To execute arithmetic and logic operations, ALU 52 includes a content-addressable memory (CAM) 54 that includes, e.g., thirty-two entries (i.e., entry 0 – entry 31) that are capable of being used by the packet

engine threads to execute microblocks stored in control store 50." [Specification, page 8, lines 3-7].

Inventive features of claim 24 include a first group of memory entries being accessible in parallel and selectable independent of a second group of memory entries in the CAM that is accessible in parallel. "CAM 54 allows the entries to be accessed in parallel so that all or some of the entries can be checked during the same time period (e.g., clock cycle) to determine if particular data is present in one of the entries." [Specification, page 8, lines 7-12]. "The CAM manager 58 is capable of partitioning individual entries into two or more subentries that are individually selectable for use in parallel comparisons. By producing subentries, particular ones of the subentries are grouped for storing one type of data (e.g. MAC addresses) and selected for use in comparing the data in parallel." [Specification, page 22, line 22 to page 23, line 3.

(6) Grounds of Rejection to be Reviewed on Appeal

Claims 1-26 stand rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement.

Claims 1-26 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement.

Claims 1-26 stand rejected under 35 U.S.C. § 101 for lack of utility.

(7) Argument

Enablement

According to *In re Wright*, the examiner has the initial burden to establish a reasonable basis to question the enablement provided for the claimed invention.[1] A patent need not teach, and preferably omits, what is well known in the art.[2] The amount of guidance or direction needed to enable the invention is inversely related to the amount of knowledge in the state of the

[1] *In re Wright*, 999 F.2d 1557, 1562, 27 USPQ2d 1510, 1513 (Fed. Cir. 1993) (examiner must provide a reasonable explanation as to why the scope of protection provided by a claim is not adequately enabled by the disclosure).
[2] *In re Buchner*, 929 F.2d 660, 661, 18 USPQ2d 1331, 1332 (Fed. Cir. 1991); *Hybritech, Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 1384, 231 USPQ 81, 94 (Fed. Cir. 1986), cert. denied, 480 U.S. 947 (1987); and *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1463, 221 USPQ 481, 489 (Fed. Cir. 1984).

art as well as the predictability in the art.[3] The "amount of guidance or direction" refers to that information in the application, as originally filed, that teaches exactly how to make or use the invention. The more that is known in the prior art about the nature of the invention, how to make, and how to use the invention, and the more predictable the art is, the less information needs to be explicitly stated in the specification.

Written Description

The inquiry into whether the description requirement is met must be determined on a case-by-case basis and is a question of fact.[4] A description as filed is presumed to be adequate, unless or until sufficient evidence or reasoning to the contrary has been presented by the examiner to rebut the presumption.[5] The examiner, therefore, must have a reasonable basis to challenge the adequacy of the written description.[6]

It is well accepted that the description requirement may be satisfied by the original claims or any other portion of the originally filed specification.[7]

Utility

Deficiencies under the "useful invention" requirement of 35 U.S.C. 101 will arise in one of two forms. The first is where it is not apparent why the invention is "useful." This can occur when an applicant fails to identify any specific and substantial utility for the invention or fails to disclose enough information about the invention to make its usefulness immediately apparent to those familiar with the technological field of the invention.[8] The second type of deficiency arises

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[3] *In re Fisher*, 427 F.2d 833, 839, 166 USPQ 18, 24 (CCPA 1970).
[4] *In re Wertheim*, 541 F.2d 257, 262, 191 USPQ 90, 96 (CCPA 1976).
[5] See, e.g., *In re Marzocchi*, 439 F.2d 220, 224, 169 USPQ 367, 370 (CCPA 1971).
[6] See *Fonar Corp. v. General Electric Co.*, 107 F.3d 1543, 1549, 41 USPQ2d 1801, 1805 (Fed. Cir. 1997) ("As a general rule, where software constitutes part of a best mode of carrying out an invention, description of such a best mode is satisfied by a disclosure of the functions of the software. This is because, normally, writing code for such software is within the skill of the art, not requiring undue experimentation, once its functions have been disclosed. * * * Thus, flow charts or source code listings are not a requirement for adequately disclosing the functions of software.").
[7] See *In re Koller*, 613 F.2d 819, 204 USPQ 702 (CCPA 1980) (original claims constitute their own description); accord In re Gardner, 475 F.2d 1389, 177 USPQ 396 (CCPA 1973); accord *In re Wertheim*, 541 F.2d 257, 191 USPQ 90 (CCPA 1976).
[8] *Brenner v. Manson*, 383 U.S. 519, 148 USPQ 689 (1966); See also *In re Ziegler*, 992 F.2d 1197, 26 USPQ2d 1600 (Fed. Cir. 1993).

in the rare instance where an assertion of specific and substantial utility for the invention made by an applicant is not credible.

The M.P.E.P. sets forth guidelines for the examiner to use in reviewing the utility requirement.[9]

(1) Claims 1-26 are enabled by Appellant's specification within the meaning of 35 U.S.C. 112, first paragraph.

Claim 1

In rejecting claims 1-26 under 35 U.S.C. §112, first paragraph as failing to comply with the enablement requirement, the examiner states with respect to claim 1 that:

> **4. Claim 1 recites the limitation "partitioning a memory device to produce a first group of memory entries being accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in parallel. The specification does not disclose how a memory device is partitioned to produce the groups recited in claim 1.**

By way of explanation, the Examiner quotes from page 8 lines 7-9 of the specification which states: "CAM 54 allows the entries to be accessed in parallel so that all or some of the entries can be checked during the same time period." The examiner argues that "This does not teach or suggest the limitations of claims 1, 8, 15, 18, 21, or 24 cited supra. This behavior is known to one of ordinary skill in the art. In a CAM, all of the data entries are compared to a data item submitted to the CAM to determine if the CAM holds a matching data item." The examiner then argues that: " It is not known to one of ordinary skill in the art how a CAM can be partitioned such that a first group of memory entries is selectable independent of a second group of memory entries. In a typical CAM, all entries are compared to the submitted data item. It is not known to one of ordinary skill in the art how a CAM can be partitioned such that one group

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[9] MPEP 2107 I (B) sets forth guidelines for the examiner in determining the utility requirement.

> Review the claims and the supporting written description to determine if the applicant has asserted for the claimed invention any specific and substantial utility that is credible.
> (1) If the applicant has asserted that the claimed invention is useful for any particular practical purpose (i.e., it has a "specific and substantial utility") and the assertion would be considered credible by a person of ordinary skill in the art, do not impose a rejection based on lack of utility.
> (i) A claimed invention must have a specific and substantial utility. This requirement excludes "throw-away," "insubstantial," or "nonspecific" utilities, such as the use of a complex invention as landfill, as a way of satisfying the utility requirement of 35 U.S.C. 101.

is selectable in parallel independent of a second group, and such partitioning is not disclosed in the specification of the instant application."

Appellant disagrees that the claimed partitioning is not disclosed in the specification, and further contends that the examiner deliberately ignores the teachings in the specification when arriving at this conclusion. Clearly, appellant's specification describes that:

> The CAM manager 58 is capable of partitioning individual entries into two or more subentries that are individually selectable for use in parallel comparisons. By producing subentries, particular ones of the subentries are grouped for storing one type of data (e.g. MAC addresses) and selected for use in comparing the data in parallel. Other subentries in the same CAM entries are grouped for storing and comparing another type of data (e.g., IP addresses). Thus, CAM 54 is configured by CAM manager 58 for storing two or more types of data in subentries that are individually selectable for use in parallel comparisons. By configuring CAM 54 for storing and comparing different types of data, the CAM 54 does not need to be loaded at separate instances with different types of data (e.g., MAC addresses, IP addresses) to perform parallel comparisons with different data types. By reducing the number of instances that the CAM entries are loaded, clock cycles are conserved that can be used to execute other operations in packet engine 48 and the network processor 28.

How partitioning is accomplished is clearly described and enabled by how the CAM manager accomplishes partitioning of the memory. Specifically, the specification provides: "By producing subentries, particular ones of the subentries are grouped for storing one type of data (e.g. MAC addresses) and selected for use in comparing the data in parallel. Other subentries in the same CAM entries are grouped for storing and comparing another type of data (e.g., IP addresses). Thus, CAM 54 is configured by CAM manager 58 for storing two or more types of data in subentries that are individually selectable for use in parallel comparisons."

Appellant's specification also describes how the partitioned CAM is used and gives specific examples of how the CAM manager partitions the CAM:

> In this example, each of the thirty-two CAM 54 entries includes a 32-bit portion for storing data (e.g., MAC addresses) for comparing in parallel with other data (e.g., a MAC address associated with a received packet). Additionally, each entry includes a 9-bit portion that stores data that represents detected matches associated with the corresponding 32-bit portion of the entry…[10]
>
> Each of the entries in CAM 54 is configurable by a CAM manager 58 that is implemented as microcode in the control store 50 and, which is executed by the packet engine 48. The CAM manager partitions the CAM 54 into a particular number of entries. The CAM manager 58 is capable of partitioning individual entries into two or more subentries that are individually selectable for use in parallel comparisons. By producing subentries, particular ones of the subentries are grouped for storing one type of data (e.g. MAC addresses) and selected for use in comparing the data in parallel. Other subentries in the same CAM entries are grouped for storing and comparing another type of data (e.g., IP addresses). Thus, CAM 54 is configured by CAM manager 58 for storing two or more types of data in subentries that are individually selectable for use in parallel comparisons. By configuring CAM 54 for storing and comparing different types of data, the CAM 54 does not need to be loaded at separate instances with different types of data (e.g., MAC addresses, IP addresses) to perform parallel comparisons with different data types.[11]

Additional examples of how this CAM is partitioned and used are set out throughout Appellant's specification.[12] Various partitions of entries and sub-entries are depicted in Appellant's FIGS. 3-7.

Memory partitioning is generally known in the art as the examiner acknowledges.[13] Claim 1 recites a particular configuration of a memory partition, namely "partitioning a memory device to produce a first group of memory entries being accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in

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[10] Appellant's specification page 9, lines 8-15.
[11] Applicant's specification, page 9, line 18 to page 10, line 12.
[12] For the sake of brevity Appellant has not reproduced additional details and examples of how the CAM is configured by the CAM manager 58. However, such details and examples are found on pages 9-17 of Appellant's specification.
[13] Examiner's action June 27, 2006 page 4; examiner's action Oct. 18, 2006 page 4.

parallel." Thus, the simple answer to the Examiner's doubt is that the CAM manager provides the claimed partitioning illustrated in FIG. 3, and as recited in claim 1.

A patent need not teach, and preferably omits, what is well known in the art. *In re Buchner*, 929 F.2d 660, 661, 18 USPQ2d 1331, 1332 (Fed. Cir. 1991); *Hybritech, Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 1384, 231 USPQ 81, 94 (Fed. Cir. 1986), cert. denied, 480 U.S. 947 (1987); and *Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 1463, 221 USPQ 481, 489 (Fed. Cir. 1984). Thus, to the extent that the examiner raises any doubts as to the efficacy of Appellant's teachings, in the predictable art of computers[14], the examiner has a larger burden to carry, namely that what was not taught would be subject matter not known in the art.

Appellant contends that in view of the teachings contained in Appellant's specification, the examiner has failed to carry the initial burden to establish a reasonable basis to question the enablement provided for the claimed invention. *In re Wright*, 999 F.2d 1557, 1562, 27 USPQ2d 1510, 1513 (Fed. Cir. 1993).

The specification contains sufficient teachings of the manner and process of making and using the invention in terms that correspond in scope to those used in describing and defining the subject matter of claim 1. Therefore, the examiner must take the specification as being in compliance with the enablement requirement of 35 U.S.C. 112, first paragraph, since the examiner has not provided any reasonable basis upon which to doubt the objective truth of the statements contained in the specification.

Thus, upon reading the application as originally filed, the application would enable one skilled in the art to make and use the same. The application as originally filed provides clear guidance regarding the partitioning of a memory. Accordingly, Appellant contends that the rejection under 35 U.S.C. § 112, first paragraph is improper and should be removed.

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[14] The amount of guidance or direction needed to enable the invention is inversely related to the amount of knowledge in the state of the art as well as the predictability in the art. *In re Fisher*, 427 F.2d 833, 839, 166 USPQ 18, 24 (CCPA 1970). The "amount of guidance or direction" refers to that information in the application, as originally filed, that teaches exactly how to make or use the invention. The more that is known in the prior art about the nature of the invention, how to make, and how to use the invention, and the more predictable the art is, the less information needs to be explicitly stated in the specification.

Claim 2

Claim 2 recites that method of claim 1 further comprises: "partitioning a memory entry in the first group of memory entries into sub-entries." Appellant's specification clearly discloses and enables: "The CAM manager 58 is capable of partitioning individual entries into two or more subentries that are individually selectable for use in parallel comparisons. By producing subentries, particular ones of the subentries are grouped for storing one type of data (e.g. MAC addresses) and selected for use in comparing the data in parallel." [15]

Claim 3

Claim 3 recites that method of claim 1, further comprises: "selecting the first group of memory entries for accessing in parallel." This feature is also described and enabled by the specification[16]

Claim 4

Claim 4, which recites that the memory device is included in a multithreaded engine of a processor, is supported by "Referring to FIG. 2, network processor 28 is depicted to include features of an Intel® Internet eXchange network processor (IXP). However, in some arrangements network processor 28 incorporates other packet processor designs. This exemplary network processor 28 includes an array of packet engines 34 in which each engine provides multi-threading capability for executing instructions from an instruction set such as a reduced instruction set computing (RISC) architecture."[17]

Claim 5

Claim 5, which recites that: "…the first group of memory entries store a first type of data and the second group of memory entries store a second type of data.", is supported by: "By producing subentries, particular ones of the subentries are grouped for storing one type of data (e.g. MAC addresses) and selected for use in comparing the data in parallel. Other subentries in

[15] Specification page 9, line 22 to page 10, line 3.
[16] Id.
[17] Id. page 4, lines 4-13.

the same CAM entries are grouped for storing and comparing another type of data (e.g., IP addresses). Thus, CAM 54 is configured by CAM manager 58 for storing two or more types of data in subentries that are individually selectable for use in parallel comparisons."[18]

Claim 6

Claim 6, which recites that: "…the memory entry includes at least two subentries.", is supported by: "Thus, CAM 54 is configured by CAM manager 58 for storing two or more types of data in subentries that are individually selectable for use in parallel comparisons." [19]

Claim 7

Claim 7, which recites that: "…the memory entry includes a combination of subentries.", is supported at least by: "CAM 60 represents CAM 54 configured by CAM manager 58 so that each CAM entry (e.g., entry 0 – entry 15) includes two subentries that store two different types of data."[20]

Claims 8-26 are supported in an analogous fashion.

(2) Appellant's specification provides a proper written description of Claims 1-26 within the meaning of 35 U.S.C. 112, first paragraph.

The Examiner also rejected claims 1-26 under 35 U.S.C. §112, first paragraph as failing to comply with the written description requirement.

The application, as originally filed, disclosed an embodiment of a method covered by claims 1-7, an embodiment of a computer program product covered by claims 8-14, an embodiment of a CAM manger covered by claims 15-17, an embodiment of a system covered by claims 18-20, and an embodiment of a packet forwarding device covered by claims 21-26. Appellant's specification and original claims as filed are presumed to be adequate, unless or until sufficient evidence or reasoning to the contrary has been presented by the examiner to rebut the presumption. See, e.g., *In re Marzocchi*, 439 F.2d 220, 224, 169 USPQ 367, 370 (CCPA 1971).

[18] Id. page 9, line 24 to page 10 line 5.
[19] Id. page 10, lines 5-7.
[20] Id. page 10, lines 16-19.

The examiner, therefore, must have a reasonable basis to challenge the adequacy of the written description. The claims as filed were not substantively amended during prosecution and thus these claims, which constitute part of the written description satisfy that requriement. See *In re Koller*, 613 F.2d 819, 204 USPQ 702 (CCPA 1980) (original claims constitute their own description); accord *In re Gardner*, 475 F.2d 1389, 177 USPQ 396 (CCPA 1973); accord *In re Wertheim*, 541 F.2d 257, 191 USPQ 90 (CCPA 1976).

In the rejection the examiner stated "[a]s the specification does not describe how the CAM manager performs the partitioning of the CAM… the specification does not provide evidence that Appellant had possession of the claimed invention at the time of filing."[21] As argued above, in addition to enabling one skilled in this art, Appellant has also provided a proper written description of the subject matter covered by claims 1-26.

(3) Appellant's Claims 1-26 possess utility within the meaning of 35 U.S.C. 101.

The Examiner also rejected claims 1-26 under 35 U.S.C. § 101 for lack of utility.

The examiner has not met the burden required to challenge the presumption utility given to Appellant's invention. According to *In Re Brana*,[22] "the PTO has the initial burden of challenging the presumptively correct assertion of utility in the disclosure… Only after the PTO provides evidence showing that one of ordinary skill in the art would reasonably doubt the asserted utility does the burden shift to the applicant." One example of evidence provided by the PTO that was sufficient to overcome the presumptively correct assertion of utility was provided in *In re Swartz* in which the PTO provided several references showing that the results were irreproducible.[23] The examiner has not met this burden. In the office action mailed June 27, 2006, the examiner simply stated:

> As stated in the specification at page 11, line 19 through page 12, line 1, an un-configurable CAM is not capable of performing the claimed functions. As there is no

[21] See Office Action mailed October 18, 2006, page 13.
[22] *In Re Brana*, 51 F.3d 1560 (Fed. Cir. 1995).
[23] *In Re Swartz*, 232 F.3d 862 (Fed. Cir. 1999).

> disclosure of a configurable CAM, the disclosed invention is inoperative and therefore lacks utility.[24]

In response to the Examiner's comments, the appellant argued that the portion of the specification to which the examiner referred describes an advantage of partitioning the memory of a configurable CAM in comparison to using an un-configurable CAM.[25] The examiner then agreed with the appellant's conclusion in the final office action but maintained the rejection and stated:

> **The Examiner respectfully agrees with the Applicant's conclusion. A configurable CAM can be partitioned, and an unconfigurable CAM cannot be partitioned. However, as Applicant had not disclosed a configurable CAM, or how a configurable CAM differs from an unconfigurable CAM, Applicant has not disclosed an operative invention…**

Appellant again refers to the above quoted paragraph describing that the CAM is configured by a CAM manager 58 that is implemented as microcode in the control store 50. As used in Appellant's specification the features of the CAM that are configurable are "… each of the entries in the CAM 54… ."[26]

Accordingly, a CAM that is partition is disclosed as having configurable entries and a CAM that is not partitioned is disclosed as un-configurable, meaning that the entries in the CAM are not configured for the purposes described by Appellant, e.g., as part of MAC and IP address processing. Appellant therefore has disclosed an operative invention and the disclosure has utility.

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[24] Office Action, page 9
[25] See Reply dated September 26, 2006.
[26] Appellant's specification page 9, line 18.

Conclusion

Accordingly, it is submitted that the examiner erred in rejecting Appellant's claims under 35 U.S.C. 112, first paragraph and under 35 U.S.C. 101 and should be reversed.

Respectfully submitted,

Date: June 18, 2007

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Appendix of Claims

1. A computer-implemented method comprising:

partitioning a memory device to produce a first group of memory entries being accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in parallel.

2. The computer-implemented method of claim 1, further comprising:

partitioning a memory entry in the first group of memory entries into sub-entries.

3. The computer-implemented method of claim 1, further comprising:

selecting the first group of memory entries for accessing in parallel.

4. The computer-implemented method of claim 1 wherein the memory device is included in a multithreaded engine of a processor.

5. The computer-implemented method of claim 1 wherein the first group of memory entries store a first type of data and the second group of memory entries store a second type of data.

6. The computer-implemented method of claim 2 wherein the memory entry includes at least two subentries.

7. The computer-implemented method of claim 2 wherein the memory entry includes a combination of subentries.

8. A computer program product, tangibly embodied in a computer readable medium, the computer program product being operable to cause a machine to:

partition a memory device to produce a first group of memory entries being accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in parallel.

9. The computer program product of claim 8 being further operable to cause a machine to:

partition a memory entry in the first group of memory entries into sub-entries.

10. The computer program product of claim 8 being further operable to cause a machine to:

select the first group of memory entries for accessing in parallel.

11. The computer program product of claim 8 wherein the memory device is included in a multithreaded engine of a packet processor.

12. The computer program product of claim 8 wherein the first group of memory entries store a first type of data and the second group of memory entries store a second type of data.

13. The computer program product of claim 9 wherein the memory entry includes at least two subentries.

14. The computer program product of claim 9 wherein the memory entry includes a combination of subentries.

15. A content-addressable memory (CAM) manager comprises:

a process to partition a memory device to produce a first group of memory entries being accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in parallel.

16. The CAM manager of claim 15 further comprising:

a process to partition a memory entry in the first group of memory entries into sub-entries.

17. The CAM manager of claim 15 further comprising:

a process to select the first group of memory entries for accessing in parallel.

18. A system comprising:

a memory device capable of being partitioned to produce a first group of memory entries that is accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in parallel.

19. The system of claim 18 wherein a memory entry in the first group of memory entries is capable of being partitioned into sub-entries.

20. The system of claim 18 wherein the first group of memory entries is further capable of being selected for accessing in parallel.

21. A packet forwarding device comprising:

an input port for receiving a packet;

and output port for delivering the received packet; and

a memory device capable of being partitioned to produce a first group of memory entries that is accessible in parallel and selectable independent of a second group of memory entries in the memory device that is accessible in parallel.

22. The packet forwarding device of claim 21 wherein a memory entry in the first group of memory entries is capable of being partitioned into sub-entries.

23. The packet forwarding device of claim 21 wherein the first group of memory entries is further capable of being selected for accessing in parallel.

24. A content-addressable memory (CAM) comprising:

a first group of memory entries being accessible in parallel and selectable independent of a second group of memory entries in the CAM that is accessible in parallel.

25. The CAM of claim 24 wherein a memory entry in the first group of memory entries is capable of being partitioned into sub-entries.

26. The CAM of claim 24 wherein the first group of memory entries is further capable of being selected for accessing in parallel.

Evidence Appendix

None

Related Proceedings Appendix

None